REMARKS

Claims 1-8, 14-19, 31, and 32 are pending.

Claims 1 and 14 are amended. Support for the amendment may be found at least at page 7, line 30 to page 8, line 3.

Claims 31 and 32 were rejected as being indefinite. They are amended to clarify the intended scope of the claims. No new matter has been added.

Examiner Interview

Applicant's representative gratefully acknowledge the opportunity to discuss the advisory action and the claims with the Examiner on April 30, 2009. The rejections with respect to Intel and various claim amendments were discussed. The Examiner indicated that certain claim amendments appear to overcome Intel. Thus, Applicant has amended independent claims 1 and 14 in accordance with Examiner's suggested language to overcome the cited references.

Claim Rejections Under 35 U.S.C. §103

Claims 1-8, and 31 are rejected under 35 U.S.C. §103(a) as being unpatentable over Intel, Inc. (IA-32® Architecture Software developer's Manual, Volumes 1-2, 2002) ("Intel"), in view of U.S. Patent No. 5,420,992 to Killian ("Killian"). Applicants respectfully traverse.

Applicants respectfully submit that Intel does not disclose or suggest "wherein substantially all multi-byte aligned branch instructions are operable to access all instructions at byte aligned addresses." In the Office Action, the Examiner points to instruction "JMP-jump" and associated text as disclosing this limitation. Particular, the Office Action states:

> see Intel, Vol. 2, page 3-357 "JMP-Jump" instruction reference; page 3-358, line 1-2, "A relative offset (rel8, re116, or rel32) is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed 8-, 16-, or 32-bit immediate value."; Examiner's note: In the description of operating modes, Intel discloses a jump instruction that uses an offset corresponding to 8 bits (JMP rel8) as well as other indexing modes (rel16, rel32 et al.).

It appears that the Examiner construes the Intel description to mean that the 8-bit offset allows jumping by one byte. Applicants respectfully disagree. The JMP rel8 instruction is described as

"Jump short, relative, displacement relative to next instruction." (Intel Vol. 2, 3-357) A short jump is further described as "a near jump where the jump range is limited to –128 to +127 from the current EIP value." *Id.* The jump range includes 256 possibilities, corresponding to the 8-bit offset size. This EIP is used throughout the JMP operation examples as the instruction address[?]. The EIP value is also defined in the Intel Architecture book:

> The instruction pointer (EIP) register contains the offset in the current code segment for the next instruction to be executed. It is advanced from one instruction boundary to the next in straightline code or it is moved ahead or backwards by a number of instructions when executing JMP, Jcc, CALL, RET, and IRET instructions. (Intel Vol. 1, section 3.5, page 3-6)

Accordingly, the EIP offset and therefore the rel8 offset value denotes the number of instructions "ahead or backwards" and not a number of bytes or bits. Because all instructions are multiple bytes (16 bit or 32 bit), the EIP offsets by a number of instructions are necessarily multiple bytes. Because the JMP instruction moves the current instruction address relative to EIP only, the JMP instruction can only access instructions at multiple byte aligned addresses. Thus, Intel does not disclose or suggest "wherein substantially all multi-byte aligned branch instructions are operable to access all instructions at byte aligned addresses."

Further, it is respectfully asserted that Killian fails to cure this defect of Intel because Killian does not disclose "access all instructions at byte aligned addresses." Because neither reference discloses a circuit "wherein substantially all multi-byte aligned branch instructions are operable to access all instructions at byte aligned addresses," withdrawal of this rejection is respectfully requested.

Claims 14-19 and 32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Intel, Inc. (IA-32® Architecture Software developer's Manual, Volumes 1-2, 2002) ("Intel") in view of U.S. Patent No. 5,420,992 to Killian ("Killian") in view of Wittig et al., "OneChip: An FPGA Processor with Reconfigurable Logic" ("Wittig"). Applicants respectfully traverse.

Applicant has amended Claim 14 to recite "wherein each of the plurality of branch instructions and non-branch instructions has a multi-byte length and is operable to access all instructions at byte aligned addresses" as suggested by the Examiner.

As discussed above, Intel and Killian do not disclose "wherein each of the plurality of branch instructions and non-branch instructions has a multi-byte length and is operable to access all instructions at byte aligned addresses." Wittig does not cure this defect of Intel and Killian. Thus, claim 14 and its dependent claims are not obvious over Intel over Killian and Wittig. For at least the foregoing reasons, withdrawal of this rejection is respectfully requested.

With regard to dependent claim 18, it is submitted that Intel, alone or in combination with Killian and Solomon fails to teach the amended limitation "wherein common subcircuitry is used to handle the immediate field associated with the branch and non-branch instructions and wherein an immediate field value is maintained in units of bytes." As discussed above concerning claim 1, Intel's instructions use an immediate field maintained in units of EIP, which is multiple bytes. Killian and Wittig do not cure this deficiency. Thus, claim 18 is independently patentable over claim 14.

CONCLUSION

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. Should the Examiner believe that a telephone conference would expedite the prosecution of this application; the undersigned can be reached at the telephone number set out below.

Please charge any required fees or credit any over payments to Weaver Austin Villeneuve Sampson LLP deposit account 50-4480.

Respectfully submitted,
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